

Progress Report EFNUDAT JRA1

Digitizer data acquisition at nELBE

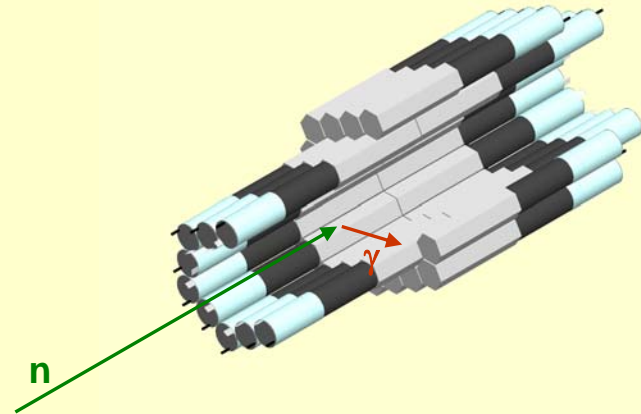
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**Forschungszentrum
Dresden Rossendorf**

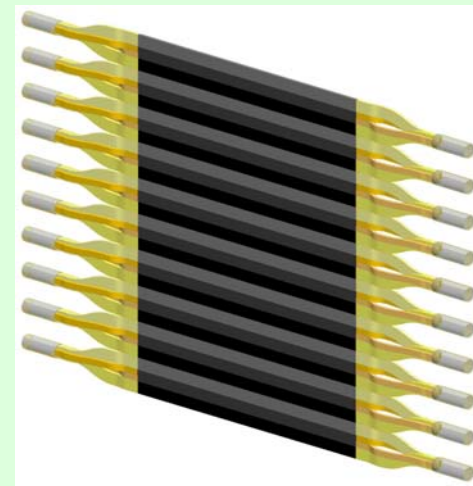
BaF₂ photon-detector array

- $l = 190$ mm
 - $\varnothing = 53$ mm
 - $\Delta\Omega$: 80 % of 4π
 - slow & fast component, pulse shape discr.
 - Inner (outer) ring 24 (18) detectors
 - Hamamatsu R2059 2" 12-stage PMTs (gain 10^7)
- ⁶⁰Co source \Rightarrow
- $\Delta E/E \approx 12$ % at 1 MeV
 - time resolution ≈ 640 ps



Plastic scintillator array for neutron detection

- $l = 1000$ mm
- Large np scattering cross section
- Good timing resolution \Rightarrow
detection point from two-sided readout
- Hamamatsu R2059 2" 12-stage PMTs (gain 10^7)
- Trigger on single photo-electron, hardware coincidence for signals from both sides gives 50 keV lower threshold for neutron detection (see talk of R. Beyer in JRA2)



2x 4 x 2 DC282 & VSYSTEMS



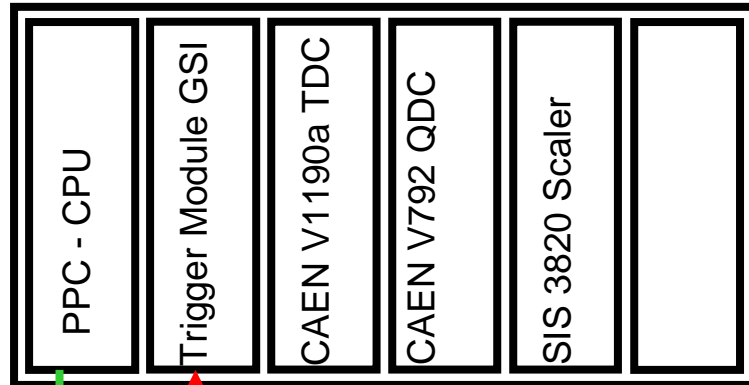
- Full waveform digitization to deal with photon-flash from bremsstrahlung and after-pulses from high-gain PMTs.
- Acqiris DC282 4ch. 2GHz 2Gs 10 bit, two crates with 32 channels in total. cPCI bus with 64bit / 66 MHz.
- Readout in SMAR mode: simultaneous read out of acquired data during acquisition into another memory segment (ping-pong mode).

JBOD

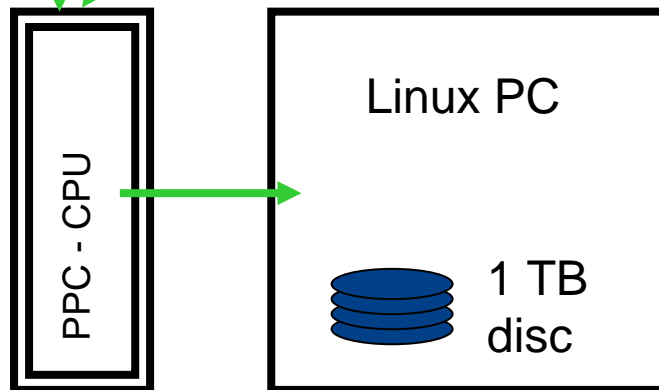
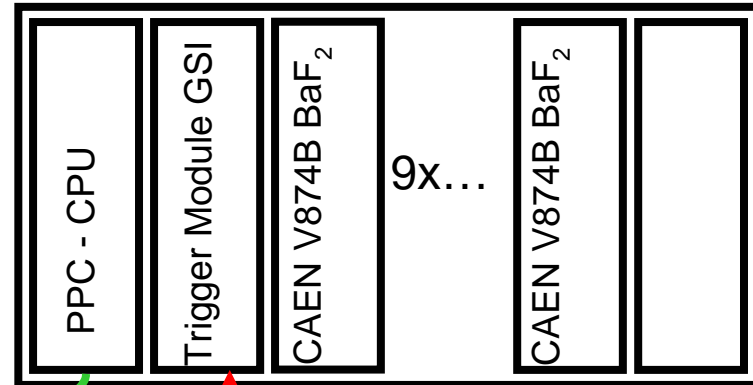


- Vsystems Recorder boards with proprietary software
- 200 MB/s continuous recording measured.
- recording on Fibre Channel JBOD with >3 TByte capacity

plastic scintillator branch



BaF₂ branch

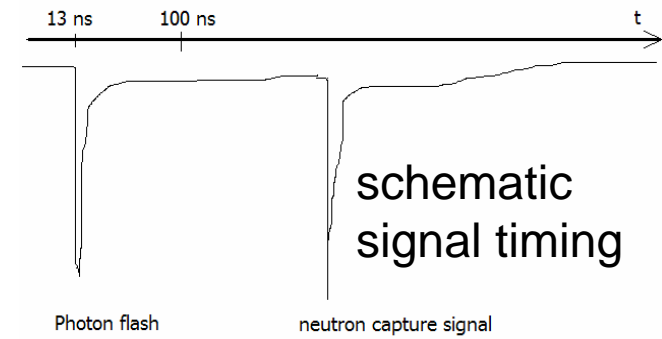


Event builder

storage

- Trigger and dead time synchronized buffered parallel readout of all channels ([GSI Multi-Branch System](#)).
- Readout dead time 80 μ s per event.
- Dedicated BaF₂ readout V874B processor from CAEN.
- Trigger-electronics developed in-house.

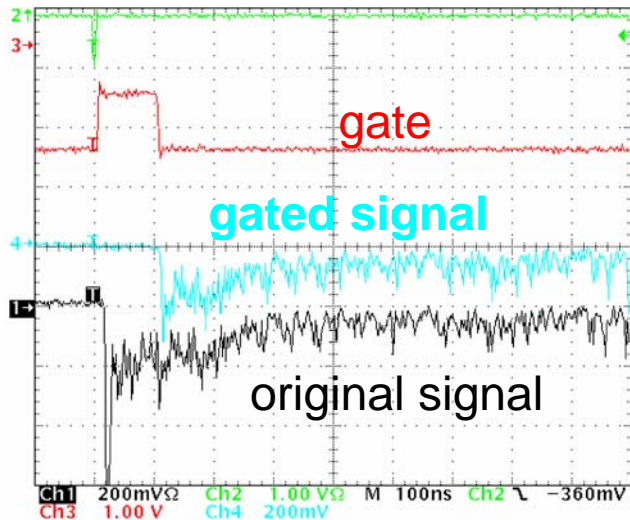
Custom electronics developed at FZD



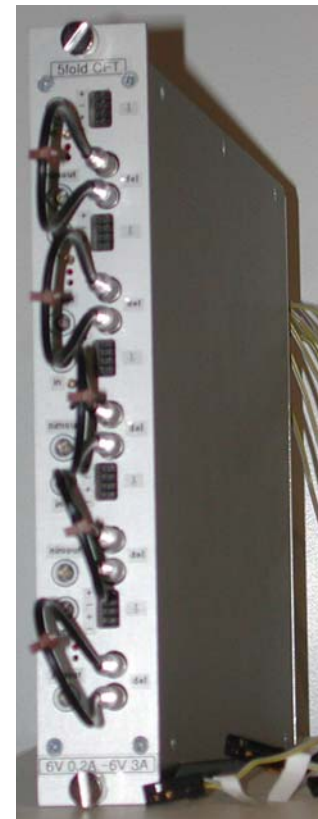
schematic
signal timing

Photon flash

neutron capture signal



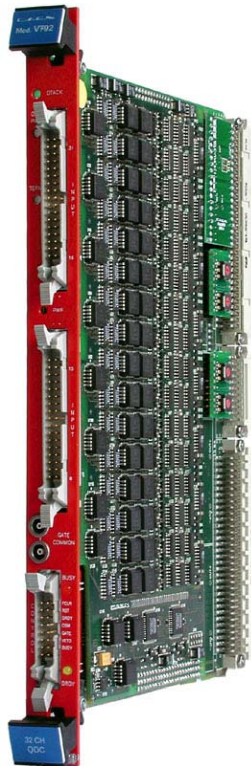
4 GHz bandwidth analog switch for
photon flash suppression of fast
BaF₂ signals



Constant-fraction
trigger with > 5 mV
threshold and ToT
output, 400 ps walk



64-fold ECL
OR and majority
module



CAEN V792 QDC

32 channels
12-bit resolution
5.7 μ s / 32 ch conversion time
Zero and overflow suppression
 $\pm 1.5\%$ differential non linearity
 $\pm 0.1\%$ integral non linearity
32 event buffer memory

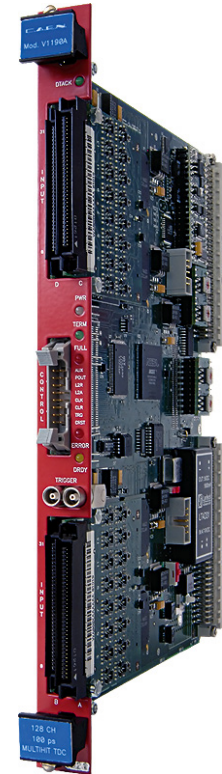
CAEN V1190a TDC

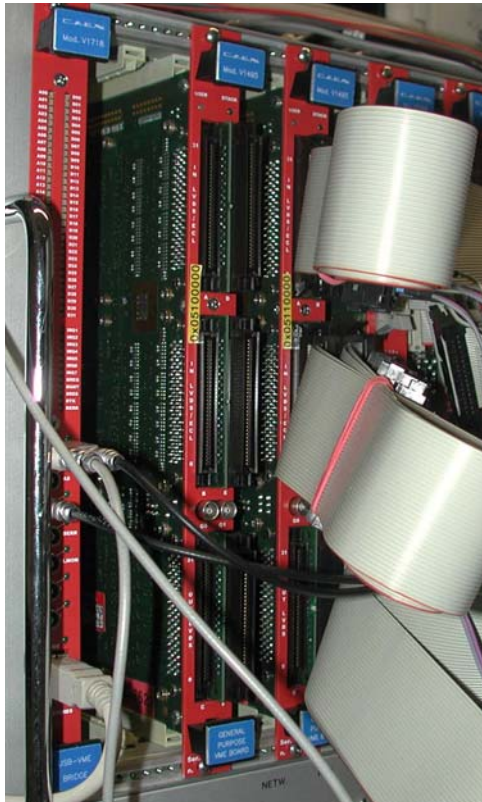
(CERN/ECP-MIC HPTDC)
128 channels ECL/LVDS
100, 200, 800 ps LSB
Leading and trailing edge detection
Continuous storage
32 k x 32 bit output buffer



CAEN V874B BaF₂ processor **(Giessen Univ. & TAPS)**

4 channels, 1 TDC, 4 QDCs, 2
Leading-edge and 1 Constant
Fraction Discriminator
11 μ s conversion time (all
channels)
Zero and overflow suppression
for each channel
32 event buffer memory





FPGA programmable trigger module CAEN V1495

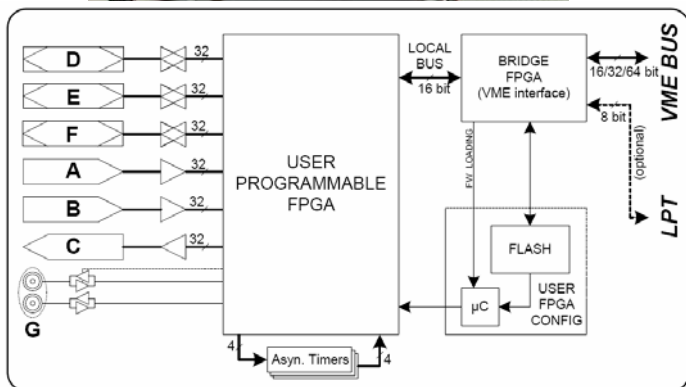
Input: 4x32 channel LVDS / ECL

Output: 2x32 channel ECL, 2xNIM/TTL

Trigger types

- 1) Plastic scintillator array, 1:N prescaled OR 2 Byte
- 2) BaF₂ array, majority selected,
1:M prescaled OR 2 Byte
- 3) Plastic & BaF₂, 1:1
- 4) Calibration test pulser, 1:1

Dead time protected operation. Programming via VME-USB interface.



ACQIRIS		VME MBS System	
		2 VME Crates	12.200 €
		3 CPUs	14.000 €
		2 GSI Trigger module	2.800 €
		2 CAEN V1190a TDC	6.000 €
		2 CAEN V792 QDC	8.600 €
		11 CAEN V874B BaF ₂	44.000 €
		1 CAEN V1495 Logic	6.400 €
		2 SIS 3800 Scaler	5.000 €
			99.000 €